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# A Review on Implementation of UART using Different Techniques

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**Abstract- Universal Asynchronous Receiver Transmitter (UART) is widely used serial data transmission protocol to support full duplex communication. UART can be implemented in a several ways according to the application required by the designer. Some of the UART contain FIFOs for the receiver or transmitter as data buffer; some of them have the 9 data bits mode and so on. This paper presents the review on such different techniques which were using with UART for reliable data transmission. The design of UART mainly consists of three kernel modules which are receiver module, transmitter module and baud rate generator playing an important role in serial communication between the UART and host CPU.**

***Keywords*- Asynchronous serial communication, Baud rate generator, Receiver, Transmitter, UART, VHDL.**

## 1. INTRODUCTION

In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback and emerges as effective method in many applications for long distance communication as it reduces the signal distortion because of its simple structure. Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. The Universal Asynchronous Receiver Transmitter (UART) is a popular and widely-used device for data communication in the field of telecommunication. It has many advantages such as simple resources, reliable performance, strong anti-jamming capability, easy to operate and realize and so on

The UART is a large scale integrated circuit which contains all the software programming necessary to fully control the serial port of a PC (Personnel computer). UART performs parallel-to-serial conversion on data character received from the host processor into serial data stream, and serial-to-parallel conversion on serial data bits received from serial device to the host processor**.** It also adds the start and stop bit to the data for synchronization. In addition to the basic job of converting data from parallel to serial for transmission and from serial to parallel on reception, a UART will usually provide additional circuits for signals that can be used to indicate the state of the transmission media and to regulate the flow of data in the event that the remote device is not prepared to accept more data.

## 2. THE UART MODULES

The UART serial communication module is divided into three sub-modules: the baud rate generator, receiver module and transmitter module Therefore, the implementation of the UART communication module is actually the realization of the three sub-modules [5].The baud rate generator is actually a frequency divider that can be calculated according to system clock frequency and the desired baud rate. The function of baud rate generator is to produce a local clock signal which is much higher than the baud rate to control the UART receive and transmit. The receiver performs serial-to-parallel conversion on the asynchronous data frame received from the serial data input. The transmitter module converts the bytes into serial bits according to the basic frame format received from the CPU. In order to synchronize the asynchronous serial data and to insure the data integrity, start, parity and stop bits are added to the serial data.

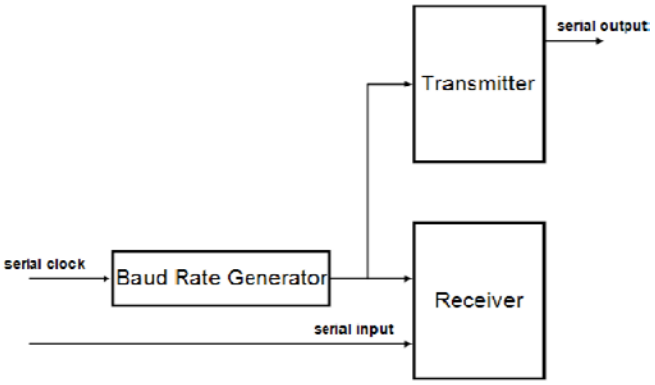


Fig. 1 UART Module

A UART has standard data frame format which consists of a start bit ‘0’, 5-8 bits data, optional parity bit and stop bit ‘1’. Fig. 2 shows the data frame format of a UART. While in idle state, serial data line will be in logic ‘1’ state. A start bit ‘0’ at the beginning of the data frame will cause a falling edge on the serial data line. This marks the detection of a data character. The idea of start bit and stop bit in UART is to achieve data synchronization. An optional parity bit can be in odd parity or even parity. Odd parity means that sum of all bits gives an odd number, while even parity means sum of all bits gives an even number. The serial data frame is shifted out with the least significant bit (LSB) first**.**

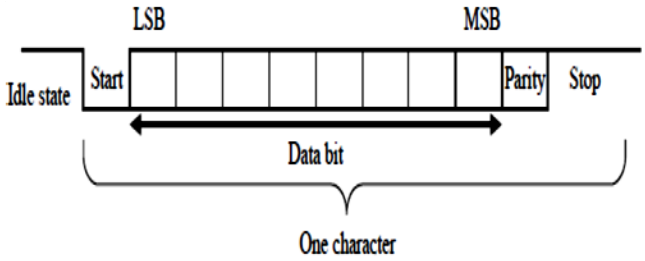


Fig.2 UART transmission protocol

## 3. DIFFERENT DESIGN APPROACHES FOR UART

From review of related work and published literature, it is observed that many researchers have designed UART by applying different techniques like algorithms, logical relations. Researchers have undertaken different methodologies with regards to UART design and its implementation on hardware platform.

### 3.1 Design of High Speed UART using VHDL

The design of the system at the gate level is become more time consuming since the integrated circuit technology is more and more complex. Therefore the use of VHDL (Very High Speed Integrated Circuit Hardware Description Language) is preferred to design such circuits especially for FPGA design. The high speed UART design achieved by describing behavior of UART circuit using VHDL [1]. Since VHDL can be used to describe and simulate the operation of digital circuits ranging from few gates to more and more complex gates. VHDL can be used for the behavioral level design implementation of a digital UART and allows describing the function of the system in a more behavioural manner, rather than focusing on its actual implementation at the gate level.

### 3.2 Multi-UART Controller

One of the most important applications of UART is Multi-channel UART Controller widely used in the field of telecommunication for achieving the high speed of transmission [3]. The proposed method presents a multi channel UART controller based on FIFO (First In First Out) technique and FPGA. In traditional universal asynchronous receiver transmitter (UART) controller, the data transmission is inefficient and the data bus utilization ratio is low. A novel design is provided to solve these problems. Multichannel UART controller improved the data transmission efficiency of normal UART ensuring that more data can be processed and transmitted in less time using the novel UART controller especially in the field of aeronautical communication. This controller can be also be used to implement communication when master equipment and slaver equipment are set at different baud Rate.

### 3.3 UART Embedded with BIST Technique

As the design systems without full testability are open to the increased possibility of product failures and missed market opportunities also to ensure the data transfer is error proof. Recently UART improves with internal diagnostic capability by the introduction of Built in Self Test (BIST) Technique and introduces status register to ensure the correctness of each incoming data [2]. The design of a UART chip with embedded built- in-self-test (BIST) architecture using FPGA technology minimized expensive tester requirements and testing procedures starting from logic circuit level to field level testing and thus improves the product reliability.

### 3.4 UART integration in OR1200

UART integration in OR1200 based SoC design proposed the idea of using IP-reusing strategy [4]. The OR1200 is a 32-bit scalar RISC with Harvard micro architecture, 5 stage integer pipeline, virtual memory support and basic DSP capabilities. The purpose of this design is to achieve data communication between OR1200 and peripheral devices through UART. This newly formed system with UART can be used as a new IP core for further application in field of high data transmission.

### 3.5 UART with Auto Tuning Baud Rate Generator and Asynchronous FIFO

In serial communication mode, detection method to determine the baud rate of data for transmission is essential. Researchers have implemented the UART with auto tuning baud rate generator and asynchronous FIFO to provide much faster operation than normal UART design [6]. UART module with auto tuning baud rate generator does not need to know the incoming data rate in advance as it automatically adjust its clock frequency with incoming data rate and proved to be one of the best detection method to determine the baud rate. Also UART employed with asynchronous FIFO as buffers can exchange the data among multiple clock domain unlike synchronous FIFOs as buffer which adjust the condition of only one clock domain. Thus UART design with auto tuning baud rate generator and asynchronous FIFO realized the speed matching between the processors and the peripherals.

### 3.6 Implementation of AES algorithm in UART Module

In the recent year, it is very important to maintain security and confidentiality of data during transmission. The cryptography plays an important role in the security of data transmission. The increasing need for protecting data communication has led to development of several cryptography algorithms. Because of the growing requirements for high speed secure communications, the researchers have proposed an application of AES algorithm in UART module which is a widely used in serial data communication to support full-duplex serial communication have been proposed [7]. This work proposes the application of Advanced Encryption Standard (AES) algorithm in Universal Asynchronous Receiver Transmitter module for secure transfer of data. The proposed architecture implements AES-128 algorithm that encrypts the data before transmission through UART transmitter and decrypts after receiving the data at UART receiver module. In this work, encryption was done by AES-128 and decryption using iterative architecture.

### 3.7 9 bit UART Module

In the recent year, a modified UART design is proposed with automatic address indication, which is called 9-bit UART [8]. In a transmission using normal UART,

every Slave devices will search every character transmitted for address byte and try to match with its unique address. This results in a lot of wasted processing time for Slave devices. In a 9-bit network, UART uses the ninth bit of a character to differentiate between an address or a data character by configuring ninth bit of UART data frame by '0' or '1' for data character and address character respectively. Using this ninth bit, Slave devices are able to distinguish an address byte, compare the address and decide whether to accept or discard the incoming data bytes. This reduces the processing time of the Slave's CPU.

## 4. CONCLUSION

This paper presents the various method used by researchers for implementation of serial communication by UART module. Most of the researchers have used VHDL language to achieve the modules of UART since VHDL makes the design implementation easier to read and understand and integrated it into the FPGA to achieve compact, stable and reliable data transmission. Thus the usage of UART can be explored using different algorithm and technique to meet the communication demands superiorly and efficiently. This design shows great significance especially in the field of embedded system, where SOC technology has recently become increasingly eminent.

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